

IDS 08/29/03

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>			Complete if Known		
			Application Number		
			Filing Date		
			First Named Inventor Philip E. MAY		
			Art Unit		
			Examiner Name		
Sheet	1	of	1	Attorney Docket Number CML00770D	

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-5495817	02-27-1998	Yamada	
		US-5790877	08-04-1998	Nishiyama et al.	
		US-6442701	08-27-2002	Hurd	
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Application Number	10/652,134
		Filing Date	3/29/2003
		First Named Inventor	May et al.
		Art Unit	2185
		Examiner Name	Daniel H. Pan
Sheet	1	of	1
		Attorney Docket Number	CML00770D

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Citation No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	r ²
h		Al-Mouhamed, M., "Lower Bound on the Number of Processors and Time for Scheduling Precedence Graphs with Communication Costs", IEEE, December 1990	
h		Samadzadeh, F. et al., "A Heuristic Multiprocessor Scheduling Algorithm for Creating Near-Optimal Schedules Using Task System Graphs", ACM, 1992	
h		Prasanna, G.N., et al., "Generalized Multiprocessor Scheduling for Directed Acyclic Graphs", IEEE, 1994	
h		Kwok, Y. et al., "Static Scheduling Algorithms for Allocating Directed Task Graphs to Multiprocessors", ACM, December 1999	

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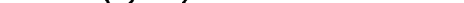

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Substitute for form 1449A/PTO				Complete if Known Application Number 10/652,134 Filing Date 3/29/2003 First Named Inventor May et al. Art Unit 2185 Examiner Name Daniel H. Pan Attorney Docket Number CML00770D	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>					
Sheet	1	of	1		

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/652,134
				Filing Date	3/29/2003
				First Named Inventor	May et al.
				Art Unit	2185
				Examiner Name	Daniel H. Pan
				Attorney Docket Number	CML00770D
Sheet	1	of	2		

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		Number - Kind Code ² (if known)				
W		3,718,912		Feb-73	Hasbrouck et al.	
W		4,128,880		Dec-78	Cray Jr.	
W		4,744,043		May-88	Kloker	
W		4,760,545		Jul-88	Inagami et al.	
W		4,807,183		Feb-89	Kung et al.	
W		4,825,361		Apr-89	Omoda et al.	
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W		5,206,822		Apr-93	Taylor	
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				Filing Date	3/29/2003
				First Named Inventor	May et al.
				Art Unit	2185
				Examiner Name	Daniel H. Pan
Sheet	2	of	2	Attorney Docket Number	CML00770D

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		Number - Kind Code ² (if known)				
U		5,697,788	Dec-97	Ohta		
U		5,717,947	Dec-98	Gallup et al.		
U		5,719,998	Feb-98	Ku et al.		
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U		6,745,160	Jun-04	Ashar et al.		
U		6,795,908	Sep-04	Lee et al.		
U		6,898,691	Mar-05	Blomgren et al.		
U		20020080795	June-02	Van Wageningen et al.		
U		20020112228	Aug-02	Granston et al.		
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U		20030128712	Jul-03	Moriwaki et al.		
U		20040003206	Jan-04	May et al.		
U		20040117595	Jun-04	Norris		
U		20050053012	Mar-05	Moyer		
U		20050055534	Mar-05	Moyer		
U		20050055543	Mar-05	Moyer		
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		Art Unit	2185
		Examiner Name	Daniel H. Pan
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		LAM, M., Software Pipelining: An Effective Scheduling Technique for VLIW Machines, Proceedings of the SIGPLAN '88 Conference on Programming Language Design and Implementation, Atlanta, Georgia, June 22-24, 1988, pp. 318-328	
		LEE, T. et al., A Transformation-Based Method for Loop Folding, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 13, No. 4, April 1994, pp. 439-450	
		KAVI, K.M. et al., A Formal Definition of Data Flow Graph Models, IEEE Transactions on Computers, Vol C-35, No. 11, Nov 1986, pp. 940-948	
		COOPER, K.D. et al., Efficient Computation of Flow Insensitive Interprocedural Summary Information, SIGPLAN Notices, Vol. 19, No. 6, June 1984, pp. 247-258	
		STRONG, H.R., Vector Execution of Flow Graphs, Journal of the Association for Computing Machinery, Vol 39, No. 1, January 1983, pp. 186-196	
		AIKEN, A. et al., Resource-Constrained Software Pipelining, IEEE Transactions on Parallel and Distributed Systems, Vol. 6, No. 12, December 1995, pp. 1248-1270	
		WULF, WILLIAM A. "Evaluation of the WM Architecture." Proceedings of the 19 th Annual International Symposium on Computer Architecture: 1992, pp. 382-390, ACM 0-89791-509-7/92/0005/0382.	
		TALLA, D., Architectural techniques to Accelerate Multimedia Applications on General-Purpose Processors, Dissertation, August 2001, pp. 94-125	
		TALLA, D., Bottlenecks in Multimedia Processing with SIMD Style Extensions and Architectural Enhancements, IEEE Transactions of Computers, August 2003, pp. 1015-1031, Vol. 62, No. 8, IEEE	

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